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## INTEGRATED STRUCTURE FOR A CONVOLUTIVE VITERBI DECODER

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

The present invention relates to an integrated circuit structure for a convolutive Viterbi decoder, and more specifically to the integrated structure for the add-compare-select units of the decoder.

#### 2. Discussion of the Related Art

Convolutive coding and decoding are used to reduce the amount of errors in digital signal transmission. In a convolutive Viterbi decoder, one add-compare-select unit (ACS) is associated with each node of a so-called "trellis". Each node of the trellis corresponds to a possible state of a shift register used in convolutive coding.

Since the present invention relates only to the interconnect structure of ACS units, it is not necessary to recall the operation of a convolutive Viterbi decoder which is well known in the art. Only those elements necessary for the understanding of the invention are described hereafter.

FIG. 1 illustrates a generic trellis for building any N-state trellis. A state  $2n$  and a state  $2n+1$  are both linked to a state  $n$  and a state  $n+N/2$ . Number  $n$  is any positive integer and numbers  $2n$  and  $2n+1$  are defined modulo-N. The links between states correspond to transitions determined by symbols received by the decoder. In this example, each symbol contains two information bits. The transitions from state  $n$  to state  $2n$  and from state  $n+N/2$  to state  $2n+1$  correspond to the reception of a symbol  $ab$ , where  $a$  is equal to 1 or 0 and  $b$  is equal to 1 or 0 according to the value of  $2n$ . The transitions from state  $n$  to state  $2n+1$  and from state  $n+N/2$  to state  $2n$  correspond to the reception of symbol  $\bar{a}\bar{b}$ .

FIG. 2 shows essential components of the ACS unit associated with state  $2n$ . This unit ACS( $2n$ ) is meant to update an associated path metric  $PM(2n)$  in a register 10 and to issue a decision  $D(2n)$ . Each path metric is a 7-bit number, for example.

Unit ACS( $2n$ ) includes an adder 12 which receives path metric  $PM(n)$  of the ACS unit associated with state  $n$  and a branch metric  $BM_{ab}$  associated, in the present example, with symbol  $ab$ . A second adder 13 receives the path metric  $PM(n+N/2)$  issued by the ACS unit associated with state  $n+N/2$  and a branch metric  $BM_{\bar{a}\bar{b}}$  associated, in the present example, with symbol  $\bar{a}\bar{b}$ .

A branch metric  $BM_x$  is a five-bit number, for example, which is smaller as the probability of having received the corresponding symbol  $x$  increases. Similarly, for a given ACS unit, the lower the value of a path metric  $PM(y)$ , the more likely it is for the received symbol to be the one corresponding to the transition of state  $y$  to the state associated with the ACS unit.

Decision  $D(2n)$  is issued by a comparator 15 receiving the outputs of adders 12 and 13. It controls a multiplexer 17 to select, from among the outputs of adders 12 and 13, that output with the lowest value. Thus, decision  $D(2n)$  indicates the most likely preceding state among states  $n$  and  $n+N/2$ . The output of multiplexer 17 is stored in register 10 as the path metric  $PM(2n)$  to be used upon receipt of the following symbol.

The ACS unit associated with state  $2n+1$  is similar to that of FIG. 2, except that adder 12 receives branch metric  $BM_{\bar{a}\bar{b}}$  and adder 13 receives branch metric  $BM_{ab}$ .

In currently used convolutive decoders, the trellis has a relatively significant size, for example of 64 states. Thus, the

interconnections between ACS units become complex and particular care is required for the positioning and routing of these ACS units on an integrated circuit so as not to occupy a large surface area and affect the operating speed.

5 An optimized solution for the positioning and routing of ACS units has been found by Sparso and is described in IEEE Journal of Solid State Circuits, Vol. 26, n° 2, February 1991, pp. 90-97, "An Area-Efficient Topology for VLSI Implementation of Viterbi Decoders and Other Shuffle-Exchange Type Structures".

10 FIG. 3 illustrates the general principle of Sparso's placing and routing. The ACS units are gathered by pairs in two columns separated by a common routing channel 20. Each pair includes, juxtaposed along the width of the corresponding column, the units associated with states  $2n$  and  $2n+1$  (modulo-N,  $n$  being any number). These two ACS units receive the path metric  $PM$  issued by the ACS unit associated with state  $n$  or with state  $n+N/2$  which is located, as shown, in a previous close pair, on the side away from the common channel 20. The missing path metric arrives to the ACS units associated with states  $2n$  and  $2n+1$  via common channel 20. There remains a local routing channel 22 between two pairs of ACS units.

15 FIG. 4 schematically illustrates an ACS network structure, obtained by using the Sparso method in the example of a 64-state trellis. The ACS units are illustrated by cells designated by the associated states.

20 The Sparso method is optimal when using integration technologies with two metallization layers. However, in more recent technologies, there are three metallization layers. When the Sparso method is transposed to a technology with three metallization layers, the size of the ACS network cannot be significantly reduced with respect to the same trellis implemented in a technology with two metallization layers.

### SUMMARY OF THE INVENTION

25 An object of the present invention is to provide an optimal integrated structure of an ACS network in a technology with three metallization layers.

30 This object is achieved by means of an integrated structure of a network of N add-compare-select (ACS) units associated with N states of a trellis of a Viterbi convolutive decoding, wherein the ACS units are physically gathered by pairs juxtaposed to form two spaced apart parallel columns, each pair including two units associated, respectively, with states  $2n$  and  $2n+1$  modulo-N, and each of which is coupled, for receiving two path metrics, to a unit associated with one of states  $n$  and  $n+N/2$  of a close pair and to a unit associated with the other of states  $n$  and  $n+N/2$  of a remote pair, the space between the two columns constituting a common channel including the interconnections between remote pairs of units. The structure is implemented in a technology with at least three metallization layers and the two ACS units of each pair are juxtaposed along the column height.

35 According to an embodiment of the present invention, the ACS units have a same topology and each pair has a link metallization topology adapted to one of the four following configurations:

- 40 (0) the unit associated with state  $2n$  is coupled to the next close pair and to the unit associated with state  $n$  of the preceding close pair;
- 45 (1) the unit associated with state  $2n+1$  is coupled to the next close pair and to the unit associated with state  $n$  of the preceding close pair;
- 50 (2) the unit associated with state  $2n$  is coupled to the next close pair and to the unit associated with state  $n+N/2$  of the preceding close pair;
- 55 (3) the unit associated with state  $2n+1$  is coupled to the next close pair and to the unit associated with state  $n+N/2$  of the preceding close pair;

(2) the unit associated with state  $2n$  is coupled to the next close pair and to the unit associated with state  $n+N/2$  of the preceding close pair; and

(3) the unit associated with state  $2n+1$  is coupled to the next close pair and to the unit associated with state  $n+N/2$  of the preceding close pair.

According to an embodiment of the present invention, each ACS unit of a pair is coupled to two groups of branch metric supply lines out of four groups of branch metric supply lines, the four groups of branch metric supply lines being common to each column.

According to an embodiment of the present invention, each ACS unit includes first to third groups of pads for establishing the connections with the next close pair and the units associated with states  $n$  and  $n+N/2$ , respectively, and fourth and fifth groups of pads for establishing connections with the two corresponding groups of branch metric supply lines, respectively, all pads being arranged according to a topology common to all units.

According to an embodiment of the present invention, the pads of each group of pads are distributed along the width of the corresponding column, the pads associated with most significant bits being on the side away from the common channel, where circuitry common to the two units of the corresponding pair is integrated.

#### BRIEF DESCRIPTION OF THE DRAWINGS

These objects, features, and advantages of preferred, non-limiting embodiments of the present invention will be described by way of example with reference to the accompanying drawings, in which:

FIG. 1 illustrates a generic trellis for building an  $N$ -state trellis.

FIG. 2 illustrates components of an ACS unit associated with state  $2n$ ;

FIG. 3 schematically illustrates the placement and routing of ACS units according to Sparso's topology;

FIG. 4 schematically illustrates an ACS structure for a 64-state trellis according to Sparso's topology;

FIG. 5 schematically illustrates four physical configurations of a group of ACS units according to an embodiment of the present invention, which constitute "assembly blocks" for realizing an ACS network according to the present invention; and

FIG. 6 schematically illustrates a structure of an ACS network obtained according to an embodiment of the present invention in the example of a 64-state trellis.

#### DETAILED DESCRIPTION

The present invention aims at optimally integrating the add-compare-select (ACS) units of a convolutive Viterbi decoder in a technology with three metallization layers. For this purpose, the invention is partially based on the Sparso structure (FIGS. 3 and 4). The Sparso structure is optimal for integration technologies with two metallization layers. However, by merely transposing this structure to a technology with three metallization layers, the occupied surface cannot be significantly reduced. In particular, the local routing channels 22 separating the pairs of ACS units in each column cannot be avoided.

According to an embodiment of the present invention, ACS unit pairs determined by the Sparso method are used, but the ACS units of each pair, instead of being juxtaposed along the width of the columns, are juxtaposed along their height. Each ACS unit is thus distributed throughout the

width of the corresponding column. As a result, the connections between the ACS units of a same pair are very short and vertical. Space is thus freed for horizontal connections and it is used for the connection of the ACS units to the path metrics PM of common channel 20. The local routing channels 22 can be practically eliminated.

The surface occupied by an ACS network according to the present invention is approximately three times lower than that of the Sparso structure. The surface reduction has the further advantage of increasing the limit operating frequency of the convolutive Viterbi decoder.

According to an embodiment of the present invention, the first ACS unit of a pair, that is, the unit which issues the path metric PM to the next close pair, corresponds to a unit on the side away from the common channel in the Sparso structure. In order to simplify the design of the integrated structure, the ACS units have a same topology. To further simplify the design, it is desirable to juxtapose column elements with the least possible concern for routing these elements.

For this purpose, the present invention provides four configurations of ACS unit pairs which, by juxtaposing them to form a column, practically establish all the links internal to the column. Thus, once a column is formed by choosing the configurations according to the pairs to be obtained, only the links external to the column practically remain to be routed, in particular those between remote pairs which go through the common channel.

FIG. 5 schematically illustrates each of these four configurations. Each ACS unit associated with state  $2n$  or  $2n+1$  of the trellis includes a pad 50 for issuing the path metric PM; a pad 51 for receiving path metric PM( $n$ ) from the unit associated with state  $n$ ; a pad 52 for receiving path metric PM( $n+N/2$ ) from the unit associated with state  $n+N/2$ ; and two pads 53 and 54 for respectively receiving the two corresponding branch metrics BM among the four possible branch metrics.

The four possible branch metrics BM00, BM01, BM10 and EM11 are distributed to all the units of a column by lines extending through the column height. The connections of pads 53 and 54 to the branch metric lines are achieved by vertical lines running out of the pairs of units where, in reduced local routing channels, they horizontally join the corresponding lines BM. This is shown for configurations 0 and 1 in which, as an example, pads 53 and 54 of unit ACS( $2n$ ) respectively receive metrics BM00 and BM11 and pads 53 and 54 of unit ACS( $2n+1$ ) respectively receive metrics BM11 and BM00.

Each path metric PM or branch metric BM is a value of several bits which is in fact associated with a group of pads distributed along the column width.

The nature of the links to be established in the local routing channels is such that the surface occupied by these local channels is negligible (approximately 5% against approximately 30% in the Sparso architecture).

The topologies of the ACS units are identical and the internal assignments of pads 50 to 54 should not be modified. The four configurations differ from one another by the metallizations which connect pads 50 through 54 to the outside. The metallizations are only shown for the connections which vary from one configuration to another. Of course, the units include other pads, for example, pads for receiving supply voltages and control and clock signals. The metallizations corresponding to those other pads, not shown, are the same for each of the four configurations, and they are designed to properly interconnect when the pairs are juxtaposed.